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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,944	11/07/2003	Gerard Boudon	FR920020012US1	2943

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
WAI, ERIC CHARLES	
ART UNIT	**PAPER NUMBER**
2195	

MAIL DATE	DELIVERY MODE
12/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/605,944	BOUDON ET AL.	
	Examiner	Art Unit	
	Eric C. Wai	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 have been presented for examination. Claim 7 was cancelled in amendment filed 10/10/2007.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms are not clearly understood in the claims:

i. Claim 1 lines 7-8 recites, "said first logic means to be presented on a dedicated bus". It is unclear how the logic means is presented.

ii. Claim 1 lines 12-14 recites, "and configured to store a valid task being presented to all of said storage fields in parallel *on* said dedicated bus". It is unclear whether the task is being stored on the dedicated bus or in the storage fields. If the valid task is to be stored in parallel on the dedicated bus, it is unclear why such storage is to be performed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Diem et al (US Pat No. 5,596,540 hereinafter Diem).

6. Regarding claim 1, AAPA teaches a FIFO based controller for slave devices attached to a processor bus of a CPU for processing tasks and storing the tasks in a FIFO memory, wherein a task consists of an address and its associated qualifying bits ([0004] lines 3-9) , the improved FIFO based controller comprising:

a first logic means for enabling valid tasks, having an address useful for at least one slave device, followed by corresponding data and for inhibiting others to be presented on a dedicated bus ([0004] lines 3-9);

a task management circuit coupled to said first logic means, said task management circuit comprising a FIFO memory connected to said dedicated bus and provided with a plurality of N storage fields forming a pile, each field being identified by a determined address and configured to store a valid task being presented (it is inherent that a FIFO based controller would have a FIFO memory with N storage fields to store task information for the slave devices).

7. However, AAPA does not teach that the FIFO memory is configured to store a valid task being presented to all of said storage fields in parallel on said dedicated bus. Diem teaches a method for writing and reading data out of a FIFO memory in a parallel manner (col 2 lines 2-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the conventional controller circuits of AAPA to utilize Diem's invention. Diem teaches that using an invention has multiple advantages such as faster frequency of operation (col 2 line 7-12) and reducing chip area (col 2 lines 12-13).

8. AAPA and Diem do not teach a second logic means that inhibit the writing of a task in the field(s) of the FIFO memory where a valid task has been entered and enable said writing in the first free field below in the pile. However, it would have been obvious to one of ordinary skill in the art to inhibit the writing of tasks to a field where a valid task has been entered. One would be motivated by the desire to not overwrite valid entries.

9. Regarding claim 2, AAPA and Diem do not teach that the first logic means comprises: a task detection circuit coupled to the processor bus that detects valid tasks; and, a FIFO controller coupled to said task detection circuit, said FIFO controller generates an ADD TASK signal to add new tasks to be performed in said FIFO memory, a CLEAR TASK signal that clears all tasks therefrom that have been executed when said corresponding data are available on the processor bus, and a control signal that is applied to a gating means for only enabling said valid tasks to be presented on said dedicated bus.

10. It would have been obvious to one or ordinary skill in the art at the time of the invention to include a signal to add and remove tasks from the FIFO memory. One would be motivated by the desire to signal the addition and removal of tasks for processing.

11. Regarding claim 3, AAPA and Diem do not teach a valid bit (V) stored in a register is associated to each of said N storage fields, wherein a first binary value being set in said register, means that a valid task has been entered in the corresponding field.

12. It would have been obvious to one or ordinary skill in the art at the time of the invention to use a valid bit stored in a register for each of the fields. One would be motivated by the desire to lower the access latency by using register memory to determine whether a task is valid.

13. Regarding claim 4, AAPA and Diem do not teach that the output of each pair of consecutive registers is connected to the inputs of a two-way XOR gate, so that only one output of the N-1 XOR gates is active (at "1") indicating thereby the boundary between the field(s) of the FIFO memory where a valid task has been entered and the remaining free field(s).

14. It would have been obvious to one or ordinary skill in the art at the time of the invention to connect the output of the registers to a two-way XOR gate. It is well known in the art the XOR gate is a commonly used component in logic.

15. Regarding claim 5, AAPA and Diem teach that said second logic means enables said writing in all the free fields of the FIFO memory instead of only the first free field (col 2 lines 7-12, wherein any field can be accessed in RAM).

16. Regarding claim 6, AAPA teaches the use of multiple slave devices ([0003-4]), but does not teach a slave controller coupled to said processor bus and task management circuit. It would have been obvious to one or ordinary skill in the art at the time of the invention to couple a slave controller to the processor bus and task management circuit. It is well known in the art that slave controllers are widely used in computer processing systems.

Response to Arguments

17. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric C. Wai whose telephone number is 571-270-1012. The examiner can normally be reached on Mon-Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EW

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 21[illegible]